Appl. No. 10/519,650

Amendment with Restriction Election and Traversal Reply to Office action of 6 December 2006

From-PHILIPS ELECTRONICS ICS

Page 2 of 6

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

- 1. (Currently amended) A mask-(12), comprising:
 - a mask substrate (14);
- a half-tone layer-(16) of half-tone mask material arranged in a pattern across the mask substrate; and
- a light-blocking layer-(48) of light blocking material arranged in a pattern across the half-tone layer;

wherein the half-tone mask material-(16) is silicon-rich silicon nitride SiN_x:H with x in the range 0 to 1.

- 2. (Currently amended) A <u>The mask according to of claim 1</u> wherein the silicon-rich silicon nitride layer (16) has a value of x in the range 0.2 to 0.6 and an optical band gap of from 2.1eV to 2.5eV.
- 3. (Currently amended) A The mask-according to of claim 1 wherein the silicon-rich silicon nitride layer-(16) has a thickness of from 40nm to 100nm.
- 4. (Currently amended) Use of a the mask-according to of claim 1 including exposing a layer of photoresist-(10) by passing ultra-violet light through the mask (12) onto the layer of photoresist-(10) to define fully removed regions-(32) in which the photoresist is fully removed, thick regions-(30) having a first thickness and thin regions-(34) having a thickness less than the first thickness in the regions exposed through the half-tone regions.

Appl. No. 10/519,650 Amendment with Restriction Election and Traversal Reply to Office action of 6 December 2006

From-PHILIPS ELECTRONICS ICS

Page 3 of 6

(Currently amended) A method of manufacture of a mask for use with an ultraviolet light source of predetermined wavelength, comprising:

providing a mask substrate-(14);

depositing a layer-(16) of silicon rich silicon nitride SiN_x:H with a nitrogen fraction x in the range 0 to 1 controlled to provide a predetermined band gap for partially absorbing ultra-violet light of the predetermined wavelength, and depositing an ultra-violet blocking layer-(18) on the mask substrate.

(Currently amended) A method of manufacture of a thin film device including: depositing multiple layers (6, 8) on a substrate (2);

providing a mask-(12) having a mask substrate-(14); a half-tone layer-(16) of half-tone mask material arranged in a pattern across the mask substrate; and a light blocking layer-(18) arranged in a pattern across the half-tone layer-(16); wherein the half-tone layer-(16) is of silicon-rich silicon nitride SiN_x:H with x in the range 0 to 1;

depositing photoresist-(10) on the multiple layers (6, 8) on the substrate (2); passing ultra-violet light through the mask (12) onto the layer of photoresist (10) to pattern the photoresist-(10) to define fully removed regions (32) in which the photoresist is fully removed, thick regions (30) having a first thickness and thin regions (34) having a thickness less than the first thickness in the regions exposed through the half-tone regions;

carrying out a first processing step on the fully removed regions (32); thinning the photoresist (10) to remove photoresist in the thin regions but not in the thick regions; and

carrying out a second processing step on the thin regions (34).

7. (Currently amended) A-The method-according to of claim 6 wherein the step of thinning the photoresist-(10) is carried out by an oxygen plasma etch.

Appl. No. 10/519,650 Amendment with Restriction Election and Traversal Reply to Office action of 6 December 2006

Page 4 of 6

8. (Currently amended) A-<u>The</u> method-according to of claim 6 wherein the multiple layers deposited on the substrate include a silicon nitride layer-(4), an amorphous silicon layer-(6) deposited on the silicon nitride layer and a metal layer-(8) deposited on the amorphous silicon layer;

the first processing step includes etching the metal layer-(8) and the amorphous silicon layer-(6); and

the second processing step includes etching the metal layer-(8).